<u>ogedsear.outega</u>

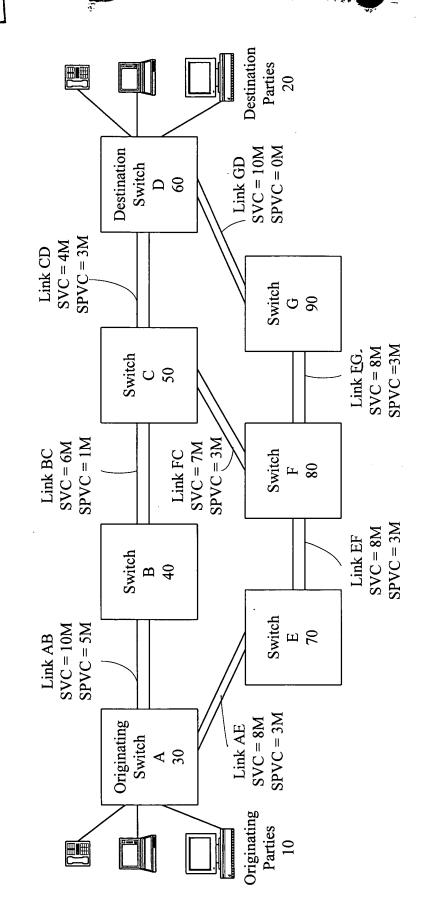
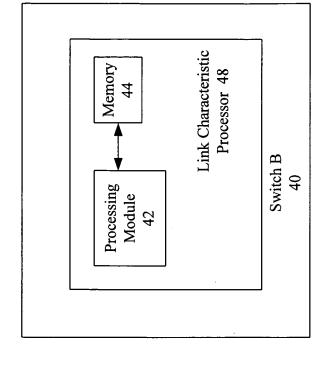


Figure 1.

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Connection Processor 38

Table 36

Figure 3.

Memory 34

Processing Module 32

Figure 2.

Originating Switch A 30



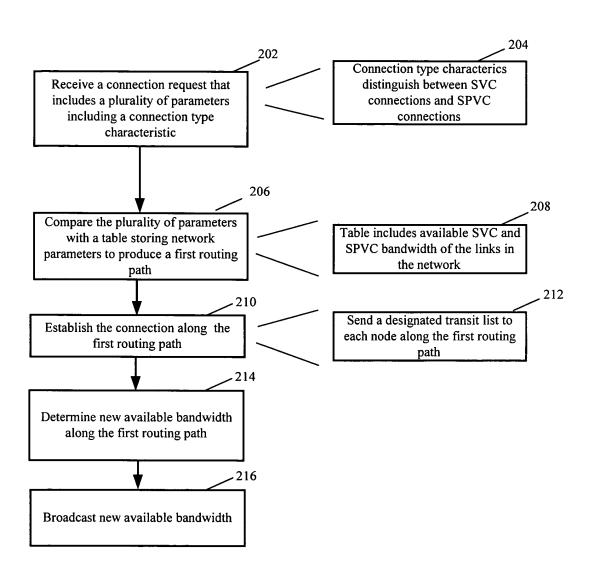


Figure 4.

J

D

I



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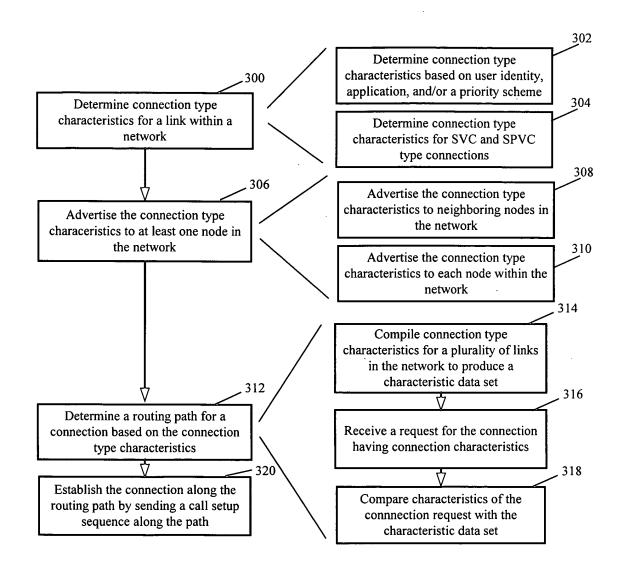


Figure 5.